Honeywell

HX5SA Structured Array Platform S150 (150nm) ASICs

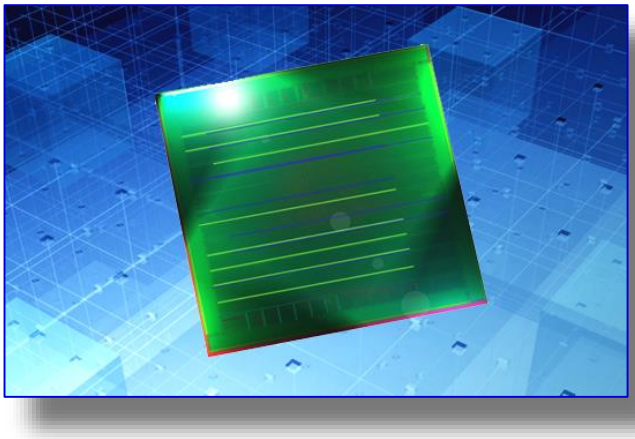
GENERAL DESCRIPTION

The Honeywell HX5SA structured array platform provides an alternative design implementation to high-end FPGAs or standard cell ASICs. By starting with a fixed array of cells and optimizing the interconnect layers for each design, the HX5SA provides a high level of integration and high performance with short lead times and cost effectiveness. This minimizes design-to-production cycle time while enabling logic designers to reap the cost and performance advantages of an ASIC implementation with minimum design resources, cost and risk.

There are currently two HX5SA arrays offering a mix of logic gates, SRAM, custom IP and I/O content. Additional array sizes and product features can be configured to support a wide range of applications. Array-specific custom packages ensure optimized power distribution, performance and radiation hardness.

HX5SA ASICs are manufactured on Honeywell's S150 150nm silicon on insulator (SOI) CMOS technology using a cell-based library and advanced ASIC design methodology. The design and manufacturing flow supports ASIC development from RTL through delivery of tested ASICs. The S150 technology is designed to withstand extremely high levels of total dose radiation and the HX5SA ASIC library flip-flops and SRAM cells are designed for low static and dynamic soft error rates (SER).

The ASIC development methodology that supports these complex ASICs is based on the Synopsys toolset. This robust design flow supports flexible design handoffs with multiple entry points including specification, RTL, or synthesized gate-level netlist.



Design for Test (DFT) is an integral part of this design flow.

Each HX5SA design is based on a proven ASIC library of standard logic elements and configurable I/O cells. Macrocells such as high-speed SERDES, phase-locked loops (PLLs) and embedded dual-port SRAMs are available. The HX5SA supports a wide variety of I/O types including LVCMOS, PCI, LVDS, SSTL, HSTL and LVPECL signaling levels. Designers can mix and match 1.8V, 2.5V and 3.3V I/O standards.

Customization of each design is accomplished by defining interconnect layers to minimize design time while providing high system performance and high routability.

This family is available with Honeywell's QML Qualified reliability and screening procedures that are fully compliant with Class V requirements.

HX5SA FEATURES

- Fabricated on 150nm silicon on insulator (SOI) CMOS
- Total dose hardness: ≥ $1x10^6$ rad (Si)
- Ultra-low Soft Error Rate (SER)
- No latch-up
- Low power
  - 17 nW/Gate/MHz (1.8V)
  - 13 nW/Gate/MHz (1.6V)
  - Usable Gates up to 6 million
- Dual-Port SRAMs
- High-speed SERDES
- PLLs (50MHz to 1.2GHz)
- VDS6 ASIC design methodology based on Synopsys tool set
- Operating voltages (nominal)
  - 1.6V or 1.8V Core
  - 1.5V, 1.8V, 2.5V and 3.3V I/O
- Operating range from -55°C to +125°C case temperature
- User-configurable I/O ≥ 500
- Configurable I/O options:
  - 1.8V/2.5V/3.3V CMOS
  - Cold spare
  - PCI
  - 2.5V, 3.3V LVDS
  - 1.8V/2.5V/3.3V SSTL
  - 1.5V HSTL
  - 3.3V LVPECL

TECHNICAL DESCRIPTION

S150 SOI CMOS Description

The Honeywell technical approach for development of HX5SA ASICs utilizes our state-of-the-art 150-nanometer SOI CMOS (S150) technology. SOI CMOS offers advantages for high-performance applications not attainable in standard bulk CMOS for radiation-hardened applications. SOI devices are fabricated in a thin film of silicon on top of a buried oxide insulator on top of a standard silicon wafer. SOI has a proven history of resistance to SEU and immunity to latch-up. These advantages simplify design steps, improve density and reduce a variety of parasitic capacitances.

Reduced Power Consumption

- SOI technology offers lower capacitance than bulk CMOS of the same feature size resulting in lower power
- 1.6V or 1.8V core operating voltage
- 1.5V, 1.8V, 2.5V, 3.3V I/O operating voltage options

HX5SA Technical Parameters

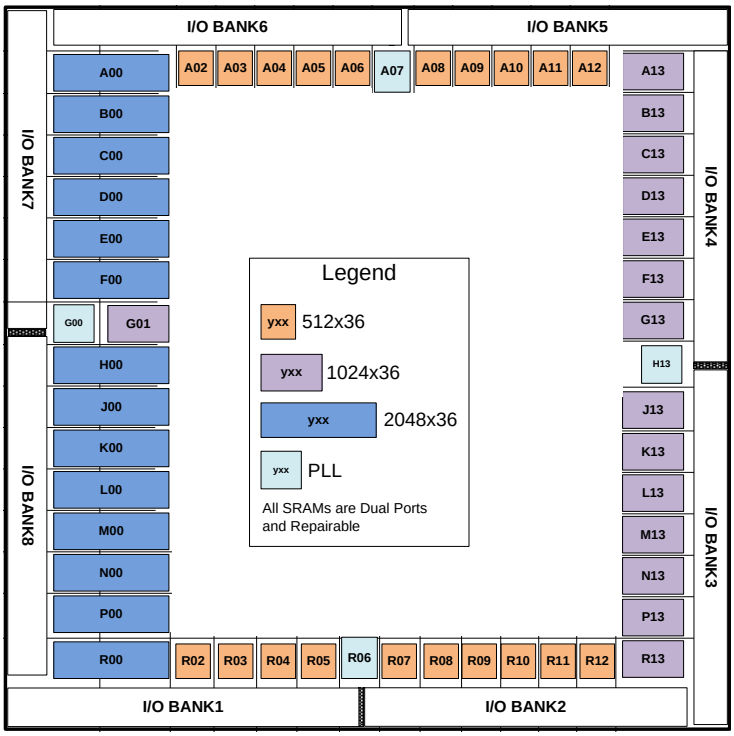
HX5SA Characteristics		Value
Minimum Geometry		0.15µm drawn / 0.11µm L_{eff}
Operating Voltage	Core Logic	1.6V or 1.8V
	I/O	1.5V, 1.8V, 2.5V and/or 3.3V
Typical Intrinsic Delay 2 Input NAND (fanout = 2)		60 ps @ 1.8V 75 ps @ 1.6V
Typical Power Dissipation, nW/Gate/MHz 20% Data, 200% Clock Activity Rate		17 @ 1.8V 13 @ 1.6V
Operating Temperature (case)		-55 to 125°C
ESD (Human Body Model)		>2000 Volts General I/O >1000V SERDES

HX5SA Resources

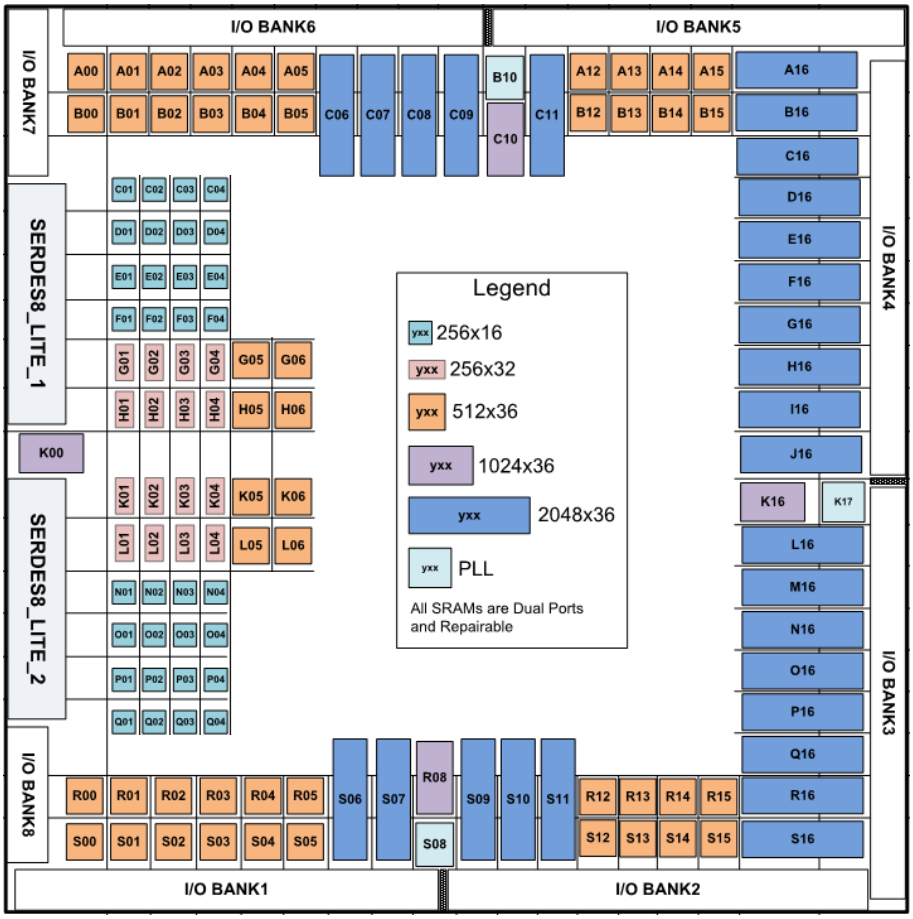
Resource	HX5SA10	HX5SA13S
Usable Gates(1)	4.5 million	6 million
SRAM bits	2 million	3.3 million
256 x 16 Dual-port SRAMs	-	32
256 x 32 Dual-port SRAMs	-	16
512 x 36 Dual-port SRAMs	20	48
1K x 36 Dual-port SRAMs	15	4
2K x 36 Dual-port SRAMs	14	28
PLLs (50MHz to 1.2GHz)	4	3
SERDES (1.0 to 3.1875 Gbps)	-	2 x 8-Lane Macrocells
I/O Signals (non-SERDES)	512	520

Notes:
(1) The number of routable gates is dependent on several factors including routing densities, amount of RAM used and I/O quantity.

HX5SA10 Floor Plan Diagram (for reference, not to scale)



HX5SA13S Floor Plan Diagram (for reference, not to scale)



RADIATION CHARACTERISTICS

Total Ionizing Radiation Dose
Total dose hardness is assured by wafer-level testing of process monitor transistors and RAM product using 10 KeV X-ray. Parameter correlations have been established between 10 KeV X-rays applied at dose rates of $1x10^5$ to $5x10^5$ rad(SiO_2)/min at 25°C and gamma rays (Cobalt-60 source) to ensure that wafer-level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation
Honeywell supports the highest levels of transient pulse radiation hardness. Please contact Honeywell for more information and specifications for applications requiring transient pulse hardness.

Neutron Radiation
SOI CMOS is inherently tolerant to damage from neutron radiation. The stated specification assumes an equivalent neutron energy of 1 MeV.

Soft Error Rate
The library elements are capable of meeting the specified soft error rates (SER) under recommended operating conditions. The specifications apply to both heavy ion and proton environments. The HX5SA library contains several types of flip-flop elements that provide options for single event effect mitigation.

Latch-up
HX5SA arrays will not latch-up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SOI substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latch-up structures.

Radiation Hardness Ratings

Parameter	Limits		Units	Environmental Conditions
Total Dose	≥ 1×10^6		Rad(Si)	
Soft Error Rate(1)(2)	Standard	Asynch.		
SEUN flip-flop	≤ 1×10^{-8}	≤ 1×10^{-8}	Upsets/bit-day	Geosynchronous orbit during solar minimum, non-flare conditions behind 100 mil aluminum shield
SEUT1 flip-flop	≤ 6×10^{-11}	≤ 2×10^{-10}		
SEUT2 flip-flop	≤ 1×10^{-11}	≤ 4×10^{-11}		
SEUT3 flip-flop	≤ 3×10^{-12}	≤ 2×10^{-11}		
SRAM (Dual-port)(3)	≤ 7×10^{-13}			
SERDES	≤ 1×10^{-12}		Bit Error Ratio	
Neutron Fluence	≥ 1×10^{14}		N/cm^2	1MeV equivalent energy

(1) Multiple types of registers with different SER ratings are available to allow optimization of ASIC speed and power.
(2) Standard – registers without asynchronous input pins, i.e., dffq, dffq_scl, dffq_syr
Asynch – registers with asynchronous input pins, i.e., dffq_ar, dffq_ash
(3) Error rates for dual port SRAM are dependent on configuration. Limits shown are for the 2048x36 configuration operating at 1.6V, 100MHz and 50% read / 50% write.

HX5SA LIBRARY

The HX5SA library contains more than 220 standard library cells with a broad array of cell types. Many logic functions have multiple versions available to allow for trade-offs of radiation tolerance, speed, power consumption and I/O drive strength. Flip-flops are available in several SEU levels to support different radiation requirements.

Embedded Phase-Locked Loops

The HX5SA arrays contain high performance embedded Phase-Locked Loop (PLL) circuits. These circuits can be used to provide frequency synthesis, insertion delay cancellation, high-frequency clock synchronization or clock multiplication on chip. The PLL operating frequency range is 50MHz to 1.2GHz.

Embedded SRAMs

The HX5SA family includes embedded SRAM blocks to efficiently implement large memory structures. The embedded SRAMs provide radiation hardness, high density and high performance in a dual-port configuration. Access to the memory data is controlled through separate read and write ports, thus providing concurrent read and write operations. SRAMs retain data content as long as power is supplied to the memory device.

The designer can implement a wider-word SRAM by connecting multiple SRAM blocks side by side, or deeper memory can be achieved by stacking multiple SRAM blocks. Typical access times are 2 to 3 ns.

The HX5SA dual-port SRAMs have separate read and write ports. Dual-port SRAMs are synchronous and use a write clock and a read clock to register inputs and outputs.

SERDES (HX5SA13S only)

To support high speed data communication needs, the HX5SA13S includes a pair of 8-lane SERDES (Serializer/Deserializer) macros. The SERDES implements the serialization and deserialization of data, clock generation and clock and data recovery of 8b10b-encoded data.

The SERDES I/O macrocell can transmit and receive date at rates of 1 - 3.125 Gbps per channel. It includes features to maximize the quality of the data transmission. To improve signal integrity and Bit Error Ratio (BER), the transmitter has 8-level programmable output drivers and the receiver has 8-level equalization. An integrated PLL provides the necessary accuracy and programmability of the internal clocks.

SERDES is capable of supporting 8b10b-encoded protocols such as Gigabit Ethernet, Serial Rapid IO, and Fibre Channel when combined with synthesized protocol functions.

SERDES Features

- Robust operation in all environments specified in the Radiation Hardness Ratings table
- Support for 8b10b-encoded protocols
- User-programmable output amplitude, pre-emphasis and equalization
- Includes RTL for insertion into design to enable manufacturing test (required)
- Bit Error Ratio ≤ 10^{-12}
- 200mW per lane (typical) at 3.125 Gbps
- Supported with 1.6V or 1.8V core voltage
- Capable of interfacing to any other SERDES through AC-coupled interface

HX5SA I/O Options

Honeywell's HX5SA family I/O cells provide a wide variety of user options for interfacing to other devices in the system. The I/O cells provide buffering and drive for signals entering or leaving the device. The HX5SA family I/O supports LVCMOS, LVDS, LVPECL, HSTL, SSTL18, SSTL2, SSTL3 and PCI signaling levels. The CMOS I/O may also suffice for many low-voltage TTL interfaces depending on specific system requirements.

The cold spare I/O feature allows a part to be powered down (VDDIO/VDD=VSS) without loading the drivers on other active parts as long as the I/Os are put in a high-Z state during power supply transitions. This can enhance overall system lifetime by enabling the replacement of parts that have become defective with redundant cold spare-equipped parts. Parts can also be powered down when not needed to minimize the degradation caused by electrical fields and/or to conserve power. This feature is an option for LVCMOS I/O and is present on LVDS inputs.

HX5SA I/O SUMMARY TABLE

Description	Operating Voltages	Operating Frequency(1)	Features
LVCMOS	1.8V, 2.5V, 3.3V	Up to ~150 MHz	Input, Output, Tri-state, Bi-directional, Cold Spare, Schmitt, Drive strength, Pad pull
PCI	3.3V	33MHz / 66MHz	Input, Output, Tri-state, Bi-directional
SSTL	1.8V, 2.5V, 3.3V	Up to 250 MHz	Class I & II, Input, Output, Tri-state, Bi-directional, Terminated or Unterminated
LVDS	2.5V, 3.3V	600 Mb/s	Input, Output, Cold Spare
LVPECL	3.3V	Up to 1.2GHz (Clock) Up to 1.2Gb/s (Data)	Input, Output, DC-coupled
HSTL	1.5V	Up to 250 MHz	Class I, Input, Output, Tri-state, Bi-directional, Terminated or Unterminated
SERDES	Core VDD (1.6V or 1.8V)	Up to 3.125 Gbps per lane	2 8-lane macrocells on HX5SA13S

Notes
1 System-level speeds depend on the off-chip signaling environment.

ASIC METHODOLOGY AND CAD TOOLS

The design flow infrastructure for HX5SA ASICs has been developed by Honeywell and Synopsys. This design environment includes:

- Leading-edge Synopsys EDA tools for designing and verifying complex ASICs
- A flexible set of front-end and back-end design services from design teams expert in the implementation of advanced ASICs and the HX5SA design flow
- Access to Honeywell intellectual property (IP), to accelerate design time and reduce development costs.

Along with support for traditional and expanded ASIC handoff options, implementation support may include design services available from Honeywell and in a fully collaborative design model.

ASIC Development Flow

The ASIC development flow processes a design from the ASIC specification through tested ASIC delivery. For ASIC designs that push the performance envelope, the flow is configured to support preliminary synthesis and place and route, termed “advanced prove-out”, to converge on an optimized design which meets all the performance constraints. The requirements associated with packaging and test are also addressed as part of the ASIC development.

Design For Test (DFT)

Honeywell has integrated Design For Test (DFT) into the HX5SA ASIC Development Flow. It encompasses memory built-in self-test (MBIST), scan/boundary scan, ATPG and functional test. It is designed to be a complete test process that allows for simulation and hardware test to use the same functional test vectors. The DFT flow is supported by tools from Mentor Graphics, Synopsys and Credence.

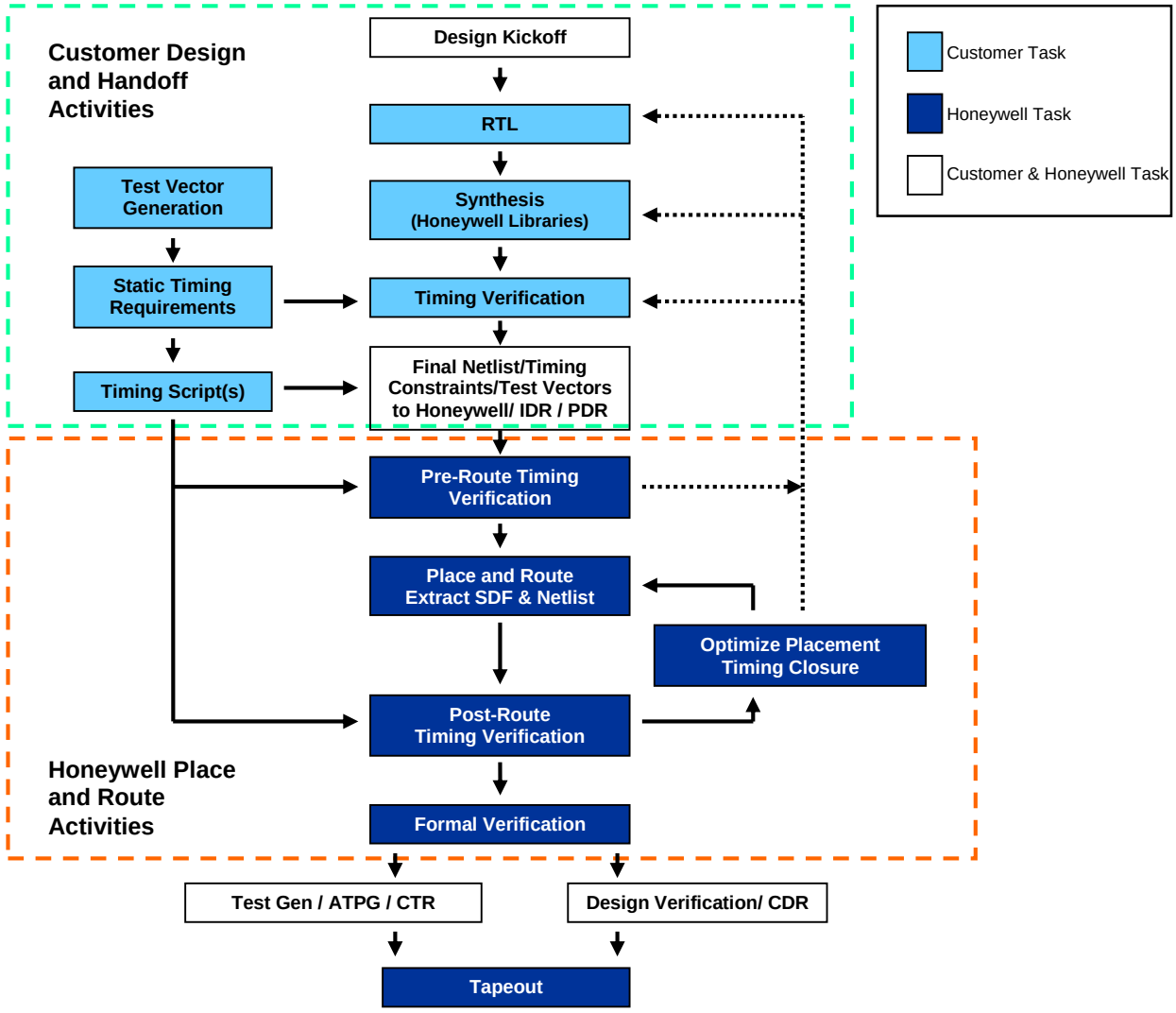
TEST CAPABILITIES

Honeywell HX5SA test capabilities include wafer- and packaged part-level testing. Testing capabilities encompass the complete Class Q and V screening flows.

HX5SA DEVELOPMENT FLOW DIAGRAM

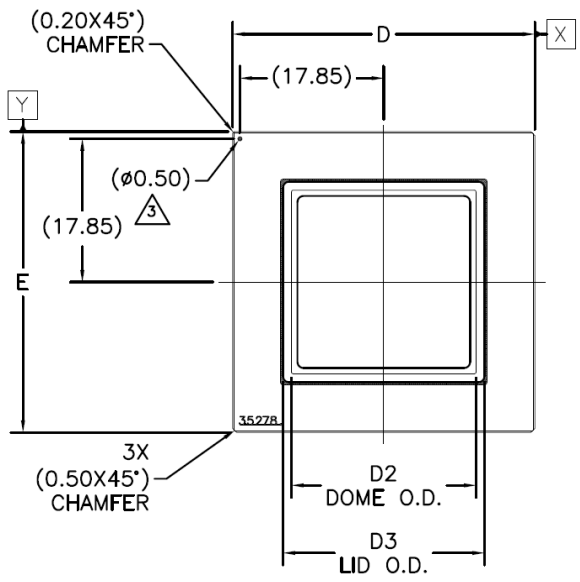
Honeywell uses an industry-standard design flow, shown in the figure below. Synthesis libraries are provided for Synopsys Design Compiler. Libraries are provided for Verilog logic simulation. Multiple entry points are available for dividing tasks between Honeywell and the customer, a common one is shown in this figure.

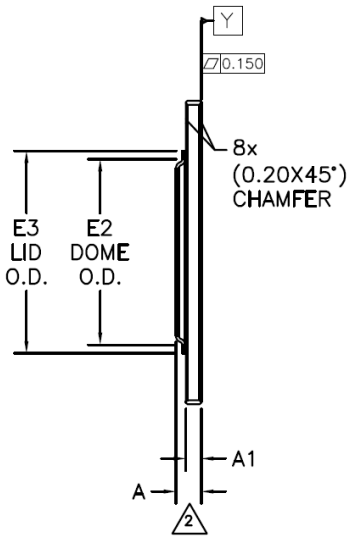
In the flow shown, the designer performs the RTL coding, synthesis, pre/post-route timing and functional verification. Honeywell performs the entire back-end layout, timing convergence and test program generation.

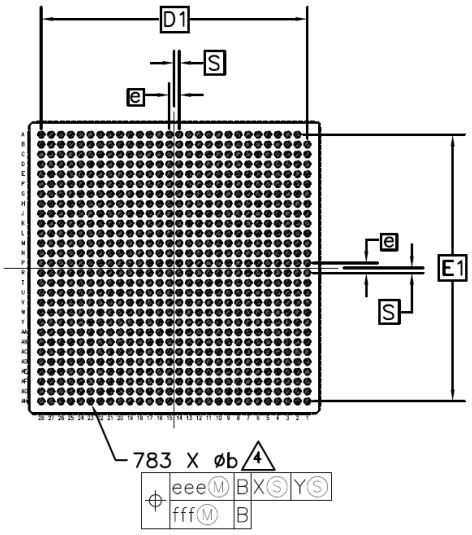


PACKAGING

A 783-pin Ceramic Land Grid Array (CLGA) is available for the HX5SA10.



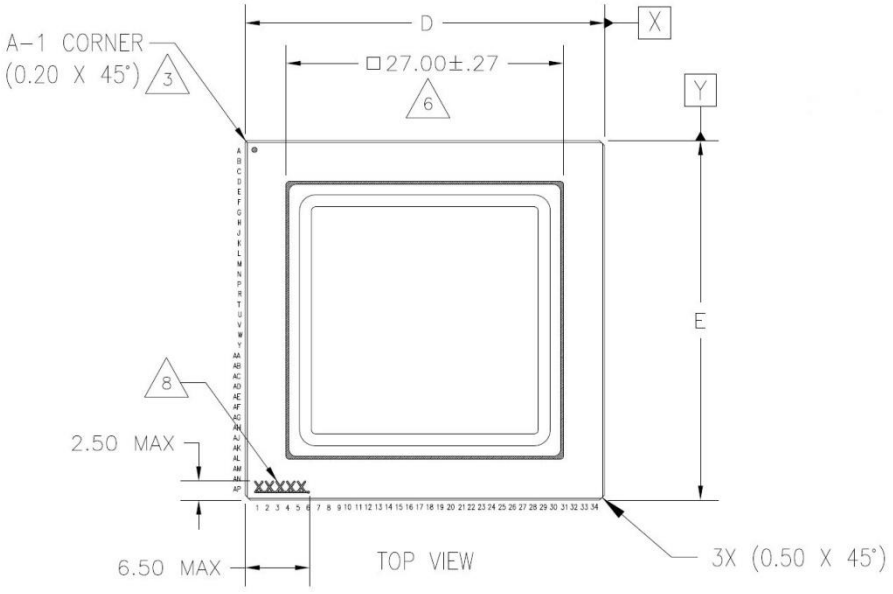


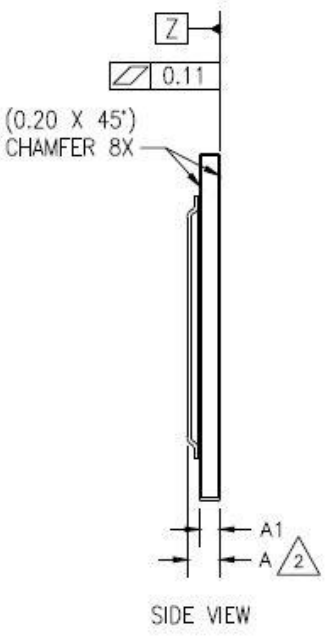


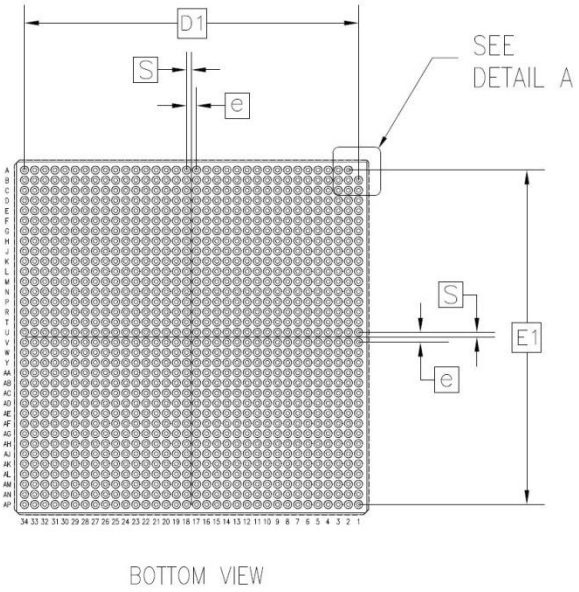
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.76	3.07	3.41	.109	.121	.134
A1	1.71	1.90	2.09	.067	.075	.082
b	0.79	0.84	0.89	.031	.033	.035
D/E	37.30	37.50	37.70	1.469	1.476	1.484
D1 E1	34.29			1.350		
D2/E2	22.78	22.92	23.04	.897	.902	.907
D3/E3	24.87	25.00	25.12	.979	.984	.989
e	1.27			0.050		
S	0.635			0.025		
eee	0.30			0.012		
fff	0.15			0.006		

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS
2. DISTANCE FROM THE BOTTOM OF THE CERAMIC TO THE HIGHEST POINT OF THE PACKAGE INCLUDES PACKAGE BODY THICKNESS A1, AND LID HEIGHT.
3. THE A–1 CORNER IS IDENTIFIED BY A SMALLER CHAMFER, AND A 0.5mm DOT ON THE TOP SURFACE, AND A MISSING LGA PAD ON THE BOTTOM SURFACE.
4. b= DIAMETER OF THE METALIZED LGA PAD

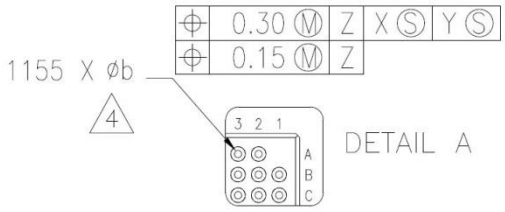
A 1155-pin Ceramic Land Grid Array (CLGA) is available for the HX5SA13S.







DIM	MILLIMETERS		
	MIN	NOM	MAX
A	2.89	3.27	3.65
A1	1.89	2.10	2.31
b	0.75	0.80	0.85
D/E	34.80	35.00	35.20
D1 E1	33.00		
e	1.00		
S	0.50		



1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS
2. DISTANCE FROM THE BOTTOM OF THE SOLDER COLUMNS TO THE HIGHEST POINT OF THE PACKAGE INCLUDES SOLDER COLUMN HEIGHT A1, PACKAGE BODY THICKNESS A2, AND LID HEIGHT.
3. THE A–1 CORNER IS IDENTIFIED BY A SMALLER CHAMFER ON THE SUBSTRATE, AN INDEX MARK ON THE TOP SURFACE OF THE SUBSTRATE, AND A MISSING LGA PAD AND COLUMN ON THE BOTTOM SURFACE OF THE SUBSTRATE.
4. b= DIAMETER OF THE SOLDER COLUMNS.
5. REFERENCE PACKAGE 58036863–001. REFERENCE LID 58036874–001.
6. PACKAGE SEAL RING OUTSIDE DIMENSIONS.
7. SOLDER COLUMN SHALL CONSIST OF 80Pb/20Sn SOLID CORE WRAPPED WITH Sn COATED COPPER RIBBON, AND OVERCOATED WITH A LAYER OF EUTECTIC 63Sn/37Pb SOLDER.
8. PACKAGE IDENTIFICATION NUMBER METALLIZED ON SUBSTRATE.

RELIABILITY

Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems for more than 25 years. Honeywell has delivered thousands of QML parts since first becoming QML qualified in 1990.

Using this proven approach Honeywell will assure the reliability of the S150 products. This approach includes adhering to Honeywell's General Manufacturing Standards for:

- Designing in reliability by establishing electrical rules based on characterization of wearout mechanisms performed on specially-designed test structures (electromigration, TDDB, hot carriers, negative bias temperature instability, radiation)
- Utilizing a structured and controlled design process
- A statistically-controlled wafer fabrication process with a continuous defect reduction process
- Individual wafer lot acceptance through process monitor testing (includes radiation testing)
- The use of characterized and qualified packages
- A thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

QUALIFICATION AND SCREENING

The test flow includes screening units with the defined flow (Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups B, C, D and E). Both the S150 process and individual product are subject to period- or lot-based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests, respectively.

Periodic qualification and testing at Honeywell and Suppliers addresses the following requirements:

Group A	General electrical tests
Group B	Mechanical - bond strength, solvents, die shear
Group C	Life tests – 1,000 hours at 125°C or equivalent
Group D	Package-related mechanical tests - dimensions, mechanical shock, vibration, acceleration, seal, temp cycle, thermal shock, moisture resistance, salt, lead integrity, lead finish adhesion, solderability, internal water vapor, solder heat
Group E	Radiation tests

Honeywell International Inc.
Aerospace Plymouth
12001 Highway 55
Plymouth, MN 55441
1-800-323-8295
http://www.honeywellmicroelectronics.com

Form #900327
April, 2016

Honeywell